

EA2402



48 Gb/s Error Analyzer, Dual 24 Gb/s Channel

The Optilab EA2402 is a Dual channel 24 Gb/s Error Analyzer (EA), combined total data rate of 48 Gb/s. Along with PG2402, this high performance analyzer unit provides up to 2X24 Gb/s error detection function for complete Bit Error Rate Testing (BERT) solutions. The user selectable reference clock allows testing BER at a specific data rate with external clock input or at a pre-defined data rate using the internal clock. An intuitive GUI, Optilab Teraport, is provided with the BERT system for ease of operation. Contact Optilab for more information.

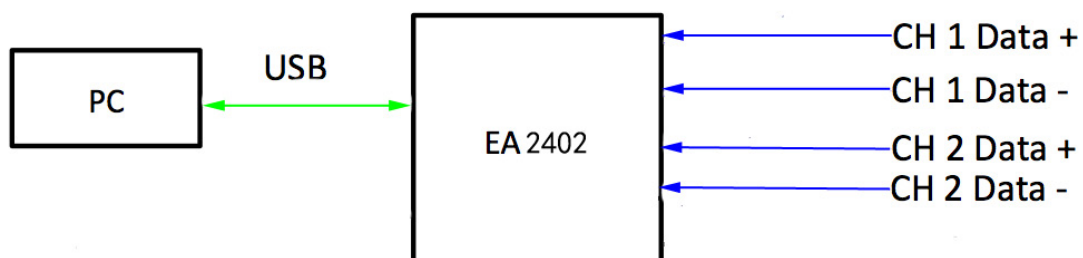
Features

- Data Rate from 2x20 to 2x24 Gbps
- PRBS of 2^7-1 or $2^{31}-1$
- Teraport GUI software included
- Deskew function

Applications

- Photonics module testing
- Electrical eye diagram to 24 Gb/s x2
- 43 Gbps DQPSK link
- 100 Gbps DP-QPSK testing

Functional Diagram



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OPTIONS

EA2402-XX

Clock:
11: External Clock Adjustment
20: 20 Gb/s fixed
24: 24 Gb/s fixed

Data Input Specifications	
Data Pattern	128 bit Fixed pattern, or PRBS (2 ⁷ -1 or 2 ³¹ -1)
Data Input Type	DC Coupled, Differential
Input Data Rate	20 Gb/s min., 24 Gb/s max.
Input Data Amplitude	0.1 Vpp min., 0.8 Vpp max.
Differential Input Impedance	100 Ω typ.
Lock Mode	Lock to ref clock or lock to data
Electrical Connectors	2.92 mm Female (K or SMA compatible)

TECHNICAL INFO

For technical info and support:

sales@optilab.com

www.optilab.com

Clock Input Specifications	
Ref Clock Input Frequency	622.5 MHz min., 750 MHz max.
Ref Clock Input Amplitude	-5 dBm min., 0 dBm typ., 3 dBm max
Recovered Clock Frequency	622.5 MHz min., 750 MHz max.
Clock Connectors	SMA female

WEB ORDER

To order, please visit OEQuest.com.



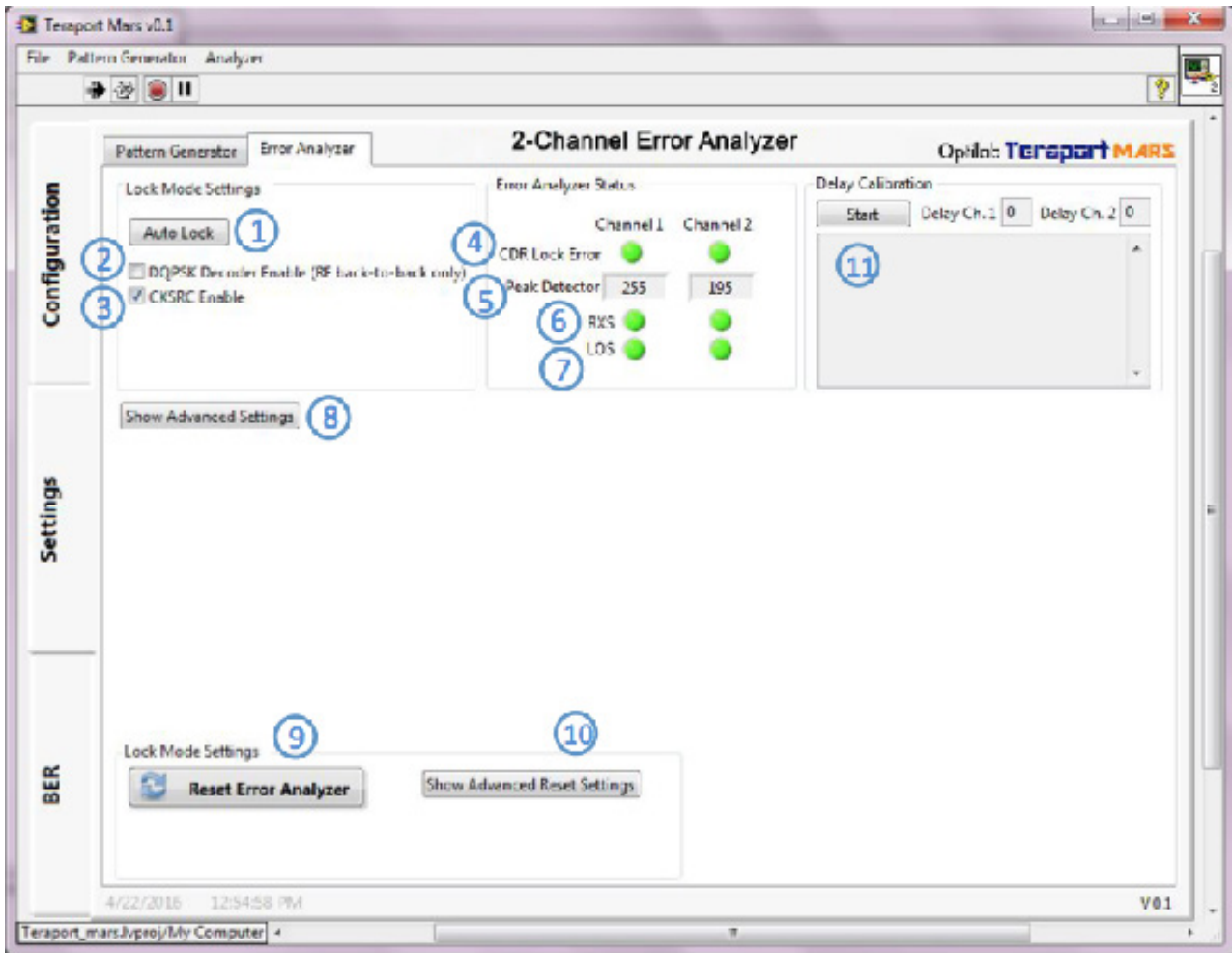
Mechanical Specifications	
Operating Temperature (standard)	0 °C to +50 °C
Storage Temperature	-40 °C to +70 °C
Power Supply Requirements	80 - 240 V, 43 - 63 Hz AC.
Power Consumption	60 W max.
Dimensions	476.6 mm x 482.6 mm x 44.5 mm

Optilab Advantage

- Innovation
- Performance
- Quality
- Customization
- Warranty

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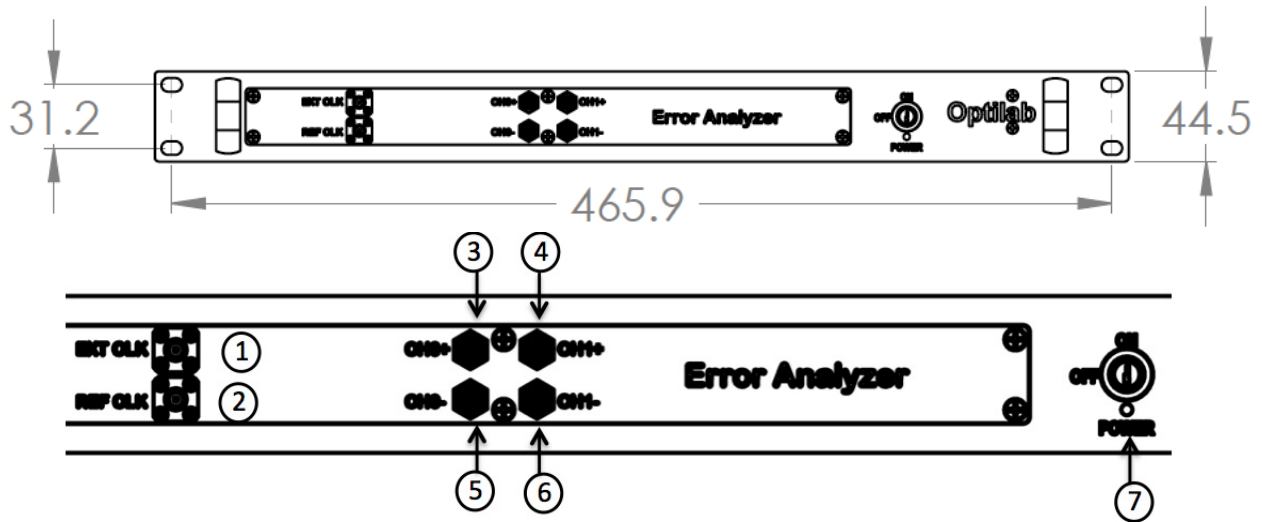
Teraport Interface



No.	Function	Description
1	Auto Lock	Automatically lock input
2	DQPSK Decoder Enable	For DQPSK only
3	CKSRC Enable	Enable recovered clock
4	CDR Lock Error	CDR lock error indicator
5	Peak Detector	Input peak detector output
6	RXS	Receiver status indicator
7	LOS	Loss of signal indicator
8	Show Advanced Settings	Menu of advanced setting
9	Reset Error Analyzer	Reset analyzer
10	Show Advanced Reset Settings	Reset advanced setting
11	Delay Calibration Start	Calibration phase delay

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Mechanical Drawing



No.	Function	Description
1	External Clock	External clock input port
2	Reference Clock	Recovered clock output port
3	CH 1+	Channel 1,data+
4	CH 2+	Channel 2,data+
5	CH 1-	Channel 1,data-
6	CH 2-	Channel 2,data-
7	Power	Turn on /off

Available Clock Rate Option

External	Adjustment from 20 Gb/s to 24 Gb/s
20G	Builtin clock for 20 Gb/s output
24G	Builtin clock for 24 Gb/s output
Custom	Any fixed clock from 622.5MHz to 750 MHz